

PREPARED BY: <i>M. Omoi</i> DATE: 11.Apr.1996	<h1>SHARP</h1> <p>ELECTRONIC COMPONENTS GROUP SHARP CORPORATION</p> <h2>SPECIFICATION</h2>	SPEC No. EC-96444
CHECKED BY: <i>M. Omoi</i> DATE: 11.Apr.1996		FILE No.
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		REPRESENTATIVE DIVISION <input type="checkbox"/> ELECTRONIC COMPONENTS DIV. <input type="checkbox"/> OPTICAL DEVICE DIV. <input type="checkbox"/> PHOTO VOLATICS DIV.

-DEVICE SPECIFICATION FOR

RF UNIT FOR DECT

MODEDL No.

RY3GH100
for portable phone

PRESENTED
BY *M. Yamada*

MI YOSH I YAM AUCH1

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Description : This specification covers RF UNIT intended for use in DECT set.

[1] GENERAL SPECIFICATIONS

1-1	Frequency range	1881.792 MHz to 1897.344 MHz
1-2	Channelization system	TDMA
1-3	Total number of channels	10 ch
1-4	Nominal antenna impedance	50 ohms
1-5	Intermediate frequency	110.592 MHz
1-6	Modulation system	GFSK Data rate: 1.152 Mbps Dev. : *288 kHz
1-7	Operating voltage	-i-B : 3.6 V ± 0.4 V PA+B1: 3.6 V * 0.4 V PA+B2: -5.0 v * 0,2 V
1-8	Absolute maximum supply voltage (Ta=25°C)	+B : 6.0 V PA+B1: 7.0 V PA+B2: < -6.0 V, > -4.0 V
1-9	Weight	26 g
1-10	Block diagram	Figure 1
1-11	PLL reference (CLOCK)	External input Freq. : 10.368 MHz Level : 100mVrms (MIN)

[2] MECHANICAL SPECIFICATIONS

2-1	Dimension and mounting details	Figure 2
2-2	Terminal details	Table 1
2-3	Wrapping details	Figure 3

[3] ENVIRONMENT SPECIFICATIONS

3-1	Operating temperature	0 °C to 40 °C
3-2	Storage temperature	-20 °C to 70 °C
3-3	Efficient humidity	Less than 85%
3-4	Storage humidity	Less than 90%

[4] TESTING CONDITIONS

4-1	Supply voltage	+B : 3.6 V ± 0.1 V PA+B1: 3.6V ± 0.1 V PA+B2: -5.0 v * 0.1 v
4-2	Ambient temperature	25 °C ± 5 °C
4-3	Ambient humidity	65 % * 10 %

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SHARP**[5] ELECTRICAL SPECIFICATIONS**

*** Measuring the following items are correspondingly to "[4] TESTIG CONDITIONS"-

*** In chart, "Y" means desired-channel

"M" means undesired-channel

"M* 1" means adjacent channel, "M± 2" means next adjacent channel

No.	Items	Specifications				Conditions
		MIN.	TYP.	MAX.	UNIT	
(TX BLOCK)						
5-1	Transmitting output power	+19.0	+22.0	+24.0	dBm	
		79.5	158	251	mW	
5-2	Emission due to modulation			8	dBm	on RF channel "Y=M±1"
				-30		"Y=M±2"
				-47		any other DECT channel
5-3	Emission due to transmitter transients			-6	dBm	on RF channel "Y=M±1"
				-14		"Y=M±2"
				-24		"Y=M±3"
				-30		any other DECT channel
5-4	Spurious emission			-36	dBm	under 1 GHz
				-30		at 1 GHz to 4 GHz
(RX BLOCK)						
5-5	Radio receiver sensitivity		-92		dBm	at B.E.R 1e-3
5-6	Radio receiver reference B.E.R			1 e-5		-
5-7	Radio receiver interference performance				dBm	desire level : -73 dBm
	<1>interfere signal strength			-83		interfere on RF channel "Y=M"
				-58		"Y=M±1"
				-39		"Y=M±2"
				-33		any other DECT channel
	<2>continuous sine wave carrier level			-23	dBm	desired sensitivity limit : +3 dB
				-43		undesired level : at B.E.R=1e-3
				-43		at 25 MHz to 1780 MHz
				-23		at 1780 MHz to 1875 MHz
5-8	Receiver intermodulation	34			dB	desire sensitivity limit : +3 dB
						undesire level : at B. E. R=1e-3
5-9	Spurious emissions when not allocated a transmit channel			-57	dBm	at 30 MHz to 1 GHz
				-47		at 1 GHz to 12.75 GHz
				-57		in the DECT band
(TOTAL BLOCK)						
5-10	PLL lock up time			380	μ sec	
i - n	Current consumption	at TX & RX		450	mA	at continuous operating
		at RX		50		



[6] PLL CHANNEL SELECTION OPERATING DATA

The data stream is clocked(on the rising edge) into the DATA input,MS B first.

6-1 Input data

<1> setting VCO division data

MSB

A6	A5	A4	A3	A2	A1	A0	N13	N12	N11	N10	N9	N8	N7	N6	N5	N4	N3	N2	N1	N0	H	L
----	----	----	----	----	----	----	-----	-----	-----	-----	----	----	----	----	----	----	----	----	----	----	---	---

● setting RX-VCO PLL data
 $D=(f_c-110,592)/1.728$

● setting TX-VCO PLL data
 $D=f_c/1.728$ f_c : RX or TX frequency (MHz)

$$D=64*N + A \quad (N>A)$$

$$A=A6*2^6+A5*2^5+ \dots +A1*2^1+A0*2^0$$

$$N=N13*2^{13}+N12*2^{12}+ \dots +N1*2^1+N0*2^0$$

● example(setting TX-VCO PLL data at 1897.344 MHz)
 $D=1897.344/1.728=1098=64N+A$
 $\therefore N=17,A=10$

MSB

A6	A5	A4	A3	A2	A1	A0	N13	N12	N11	N10	N9	N8	N7	N6	N5	N4	N3	N2	N1	N0	H	L
L	L	L	f	L	H	L	L	L	L	L	L	L	L	L	L	H	L	L	L	L	H	L

<2> setting reference division data (fixed value : R=12)

MSB

R15	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	H	H
L	L	L	L	L	L	L	L	L	L	L	L	H	H	L	L	H	H

<3> setting options

MSB

D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	L	H
L	H	H	H	※	※	L	L	L	H	H	※	※	※	L	H

except marking ※, fixed value.

D9,D8 : stand-by control bits

D9	D8	descriptions
L	L	PLL stand-by,PD output:high impedance
H	H	PLL active

▽ to be continued

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Wrapping details

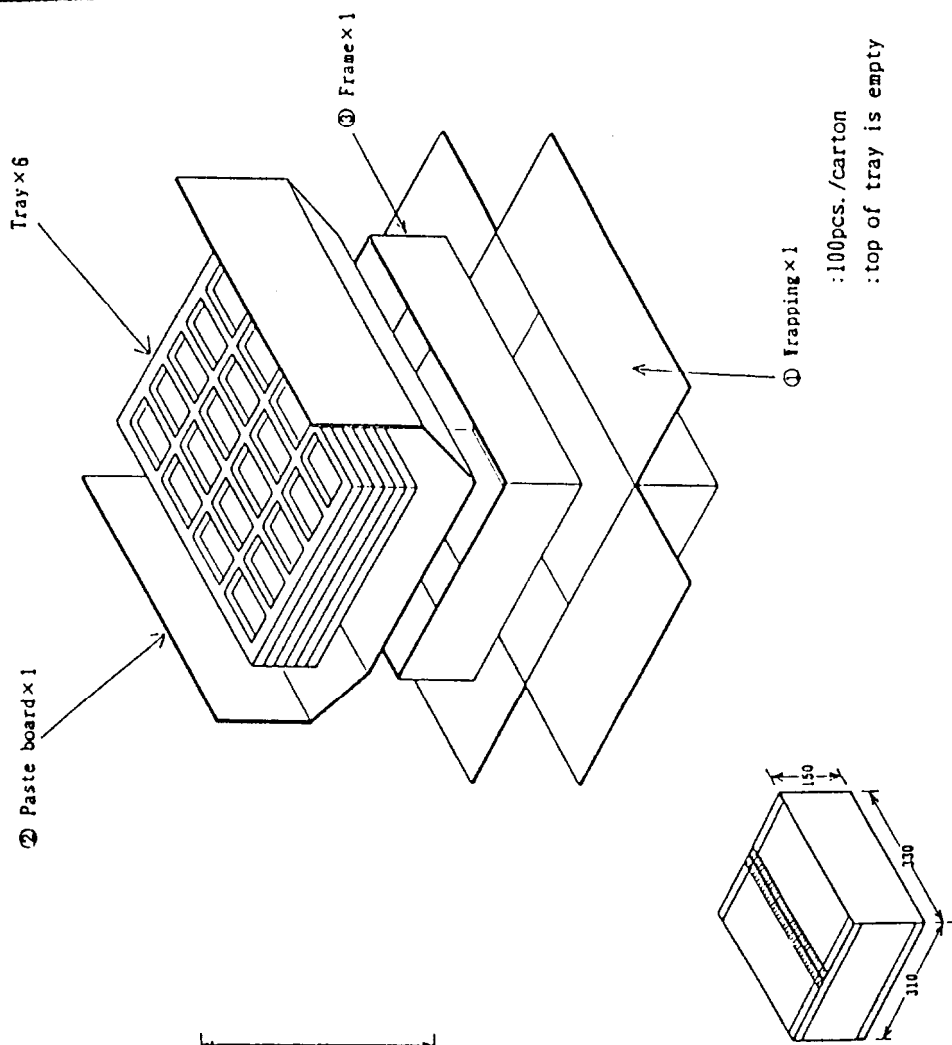
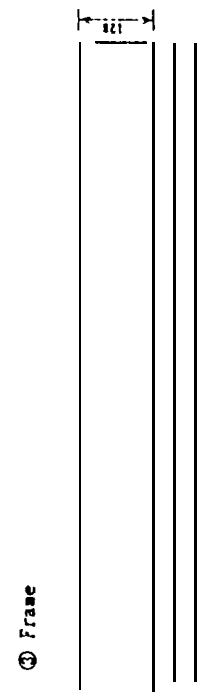
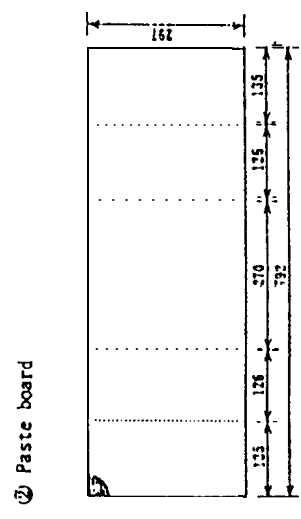
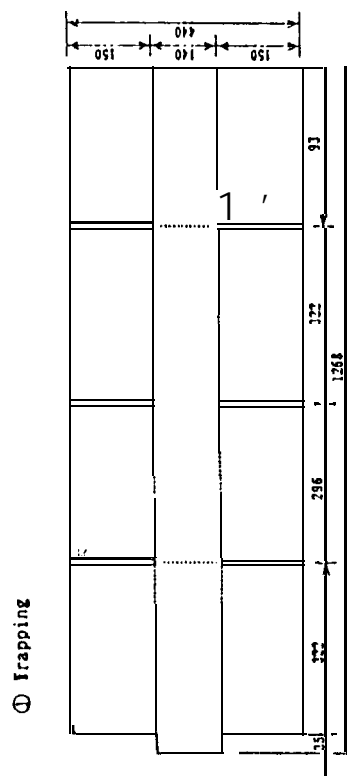


Figure 3

(Unit mm)



D2,D1,D0 : charge pump drive bits

D2	D1	D0	charge pump current
L	L	L	0.175 mA
L	L	H	0.250
L	H	L	0.350
L	H	H	0.500
H	L	L	0.700
H	L	H	1.000
H	H	L	1.400
H	H	H	2.000

We recommend that you would set the parameter with following manner;

When you want to set to “Stand-by mode” or “Channel search mode” , [hen you should set (D2,D1,D0) = (H,H,H)

On the other hand, to “other normal operating mode” , then set (D2,D1,D0) = (L,L,L)

Please be advised that,when(D2,D1,D0) =(H,H,H), PLL lock-up time is faster but C/N of VCO become worse. On the other hand, (D2,D1,D0) = (L,L,L) , PLL lock-up time is slower, however, C/N of VCO is beter.

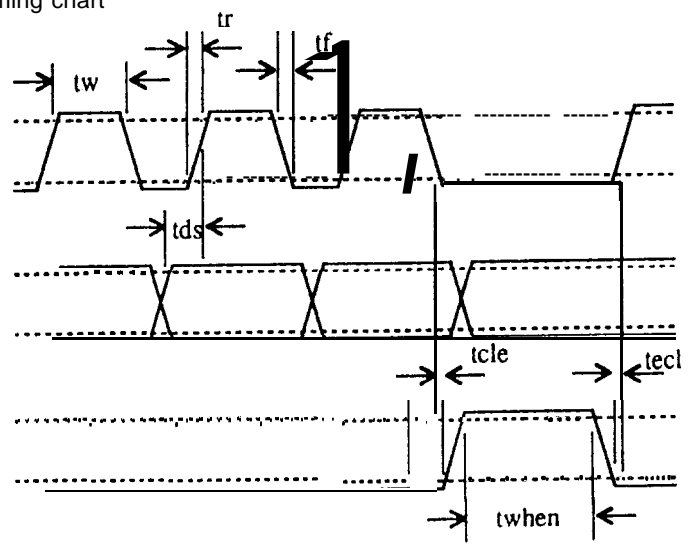
● example(setting options for RX receiving mode)

MSB

D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	L	H
L	H	H	H	H	H	L	L	L	H	H	H	H	H	L	H



6-2 Timing chart



Parameter	Symbol	Limit values		Unit
		MIN.	MAX.	
clock	fcl		10	MHz
H-pulse. width(clock)	t_w	60		ns
data setup	tds	20		ns
setup time clock-enable	tcle	20		ns
setup time enable-clock	tecl	20		ns
H-pulse. width(enable)	twhen	60		ns
rise, fall time	tr,tf		10	μs

6-3 Input voltage (DATA,CLOCK,ENABLE)

(unit: V)

input	MIN.	MAX
"H" level	+B*0.7	+B
"L" level	0	+B*0.3



◆◆◆ BLOCK DIAGRAM ◆◆◆

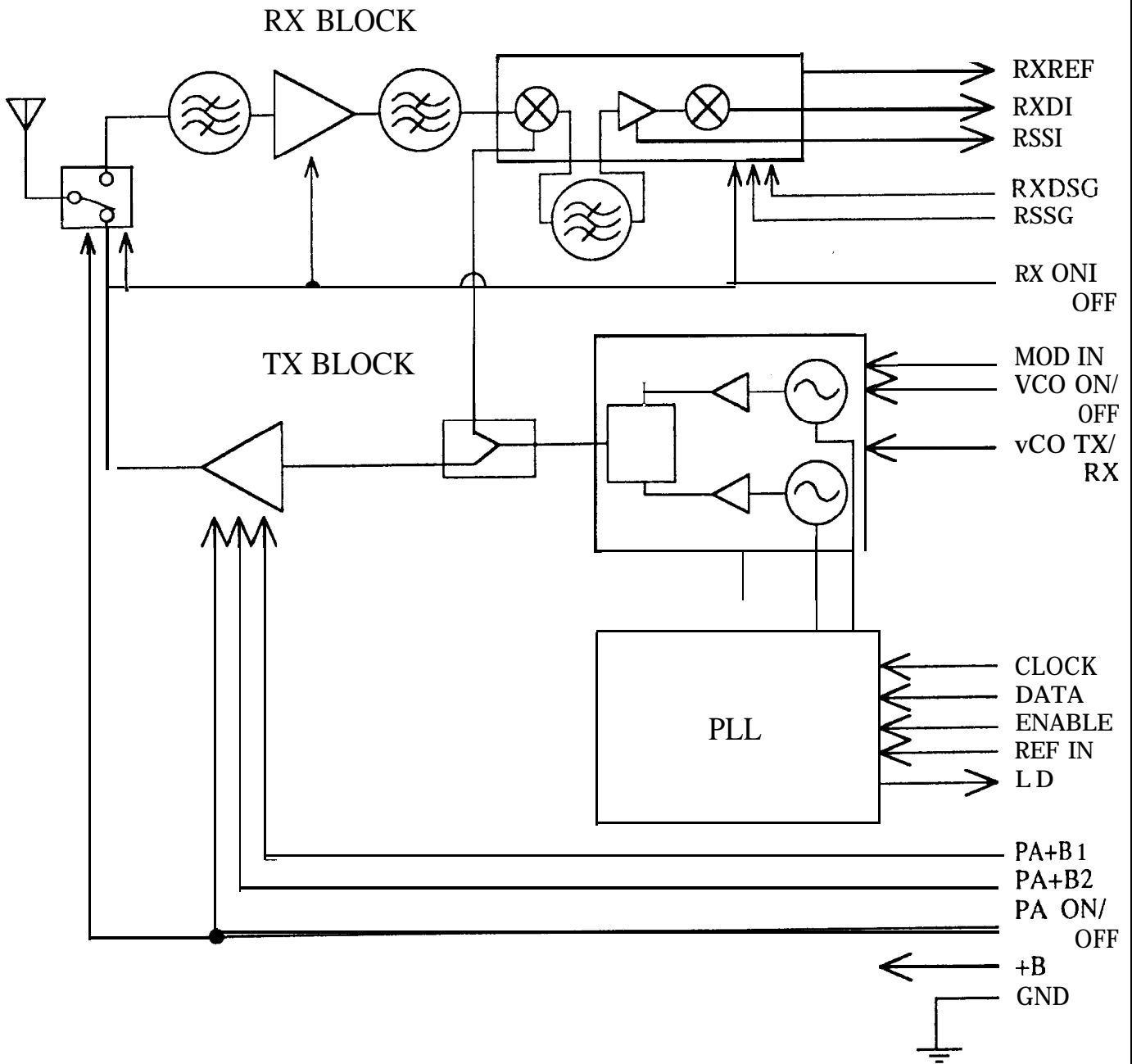


Figure 1

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◆◆◆ TERMINAL DETAILS ◆◆◆

No.	TERMINAL NAME	1/0	NOTE
1	ENABLE	1	"H": +B*0.7 +B PLL enable with internal pull-up resistor "L": 0 V +B*0.3
	REF IN	I	100 mVrms MIN. Referencesignal input (10.368 MHz)
3	CLOCK	I	"H": +B*0.7 +B PLL clock with internal pull-up resistor "L": 0 V +B*0.3
	DATA	I	"H": +B*0.7 +B PLL data with internal pull-up resistor "L": 0 V +B*0.3
5	VCO TX/RX	I	"H": 2.0 V +B TX-VCO active "L": 0 V 0.4V RX-VCO active
	+B	I	3.6 V ± 0.4 V
LD	0		0.5 mA MAX. open drainunipolar output of the phase detector in the form of a pulse-width modulated signal, "L" pulse-width corresponds to the phase difference.
8	VCO ON/OFF	- i -	"H": 2.0 V +B VCO (TX & RX) active "L": 0 V 0.4 V VCO (TX& RX) off
	MOD IN	I	"H": 3.6V ± 10% given a peak transmit frequency of (fc - 9 "L": 0V 0.4 V (fc - f)
10	PA+B2	I	-5.0 V * 0.2V Power amp. negative voltage source
11	PA+B1	I	3.6 V ± 0.4 V Power amp. positive voltage source
12	PA ON/OFF	I	"H": 2.0 V +B TX ANT-SW on/ Power amp. on "L": 0V 0.5 V RX ANT-SW on/ Power amp. off
13	GND	-	
14	RSS1	I	peak holdoutput
15	RXDI	O	I(RXDI) :370 μ A TYP. demodulated output signal,load cap< 10pf
16	RSSG	I	"H": 2.2 v +B RSSI reset mode "L": 0V 0.4 V RSSI hold mode
	RXREF	O	I(RXREF) :210 μ A reference voltage output MAX.
18	RX ON/OFF	I	"H": 2.2 V +B active mode "L": 0V 0.4 V stand-by mode,RSSG input ready RXDSG "L" required during switching in either direction.
	RXDSG	I	"H": 2.2 V +B offset sample mode (baseband DC offset compensation operates as closed loop) "L": 0 V 0.4 V offset hold mode (compensation)
20	NC		

Table 1